Journal of Engineering Technology and Sciences
Volume 02, Issue 01, January 2025 *ISSN: 3048-913X*
www.jets.org.in *DOI: https://doi.org/10.5281/zenodo.14737255*

Effects of Gate Length and Source-Drain Bias on Electron Transport Properties in SiC-Based MOSFETs

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To Cite this Article
Sneha Latha and Monish, "A Monte Carlo Analysis of the Effects of Gate Length and Source-Drain Bias on Electron Transport Properties in SiC-Based MOSFETs", Journal of Engineering Technology and Sciences, Vol. 02, Issue 01, January 2025, pp: 08-11

Abstract*: The Simulation results from ensemble Monte Carlo techniques analyze the effect of gate length along with numerous source drain voltage settings on wurtzite SiC MOSFETs properties. The electronic conditions in conduction band valleys appear using non-parabolic ellipsoidal valleys which instruct the emphasis on dominant Brillouin zone symmetries. The calculation includes the following scattering mechanisms: alloy, piezoelectric, polar optical, acoustic, and impurity. The phase-shift analysis extends beyond Born approximation to handle the scattering effects of ionized impurity scattering. Our model features two transistors with gate length dimensions of 200 and 400 nanometers. Simulations show that maintaining a constant channel length produces higher drain current output at smaller gate lengths thus resulting in greater transistor transconductance value. The reduction of drain current leads to diminished drain barrier penetration. Models predicting drain current and electrical properties show close interactions between experimental data points while using device parameters that match the experimental structure specifications.*

Keywords*: Ensemble Monte Carlo, channel length, transconductance, Brillouin zone*

I. Introduction

SiC with a broad bandgap finds applications in commercial devices through heterojunction field effect transistors (HFETs) and brilliant LEDs that operate at ultraviolet and blue and green wavelengths for sensor applications and CD-ROM use [1–3]. Tests have shown SiC can achieve exceptional peak electron velocity which provides potential benefits for high-frequency applications. Entering the high-temperature high-breakdown-voltage operating zone because this material displays low intrinsic carrier concentrations related to extensive energy gaps enables better management of free charge at various temperature levels. Transport device development using SiC materials remains inaccessible because scientists haven't properly understood fundamental transport behavior and properties. Support for further study about these materials stems from their tremendous technical possibilities. To date the MOSFET transistor emerges as the most common choice among integrated circuit builders thanks to its easy fabrication and low doping control issues and its capacity to achieve dense wiring structures [1–5].

Industrial operations continue to choose silicon as their semiconductor material while they pivot toward manufacturing wide band gap semiconductors like SiC due to their optimal electron mobility measurement potential for rapid frequency switching capabilities. Its direct bandgap characteristics create simpler optical integration possibilities. The literature shows growing interest in SiC MESFETs because researchers study their simulated behaviour to better understand their fundamental operational principles. Mobility and the potential for higher frequency operating rates. Additionally, its direct bandgap makes integration with optical equipment simpler. SiC MESFETs have so drawn a lot of interest in the literature, especially in relation to their simulation in an effort to comprehend the fundamental ideas behind how they function. SiC emerges as a primary material for optical switch construction because it delivers similar mobility attributes as other III-V compounds. The basic devices exist in simulation form but multiple researchers recognize SiC's probable important role. Research demonstrates that MOSFET devices deliver increased efficiency over traditional semiconductor devices [6–8]. The insulation nature of MOSFETs creates extremely thin transistor channel formation layers with zero sub-base current. The gate obtains better control of channel current because the carriers are located nearer to it. A complete presentation of simulation results appears in Section 2 followed by an analysis of threshold voltage behaviour and the gate length effects on drain voltage-dependent gate current curves in Section 3.

II. Research Method

An ensemble Monte Carlo simulation model predicted the electron transport behavior found in SiC MOSFET devices. The 104 super particles act as mobile proxies which track movements to reproduce charge carrier behavior in the device testing setup. Elements move through collisions in classical paths when their velocity combines with effective mass under field conditions. Random numbers enable the selection of scattering mechanisms allowing for the definition of propagation duration and other physical aspects. A self-consistent Monte Carlo simulation was achieved using an analytical band structure model that included five ellipsoidal valleys with non-parabolic features. This model considers Acoustic, polar optical, ionized impurity, piezoelectric, and nonequivalent intervalley scattering as its scattering modes. We describe the device structure features in the following way. The device consists of 8 μm x-direction length divided into two regions as 500 nm or 800 nm gates and drain. A 3 eV shottky connection represents the Au/Pt contact potential but source and drain contacts operate with ohmic behavior. An effective source-to-gate distance and gate-to-drain separation are set at 0.7 micrometers. High simulation run times become necessary in order to ensure simulator convergence because the device measurements span such large lengths. The simulation uses ambient temperature as its operating proxy.

III. Result and Analysis

The Figure 1 demonstrates that the device electric field varies according to position when source-drain voltages reach from 0 to 7 V. Both Figure 2 and this figure indicate that nearly the entire potential disappearance occurs under the gate region. Space charge nonuniformity produces a dramatic electric field shift throughout the device which reaches maximum strength near the drain end.

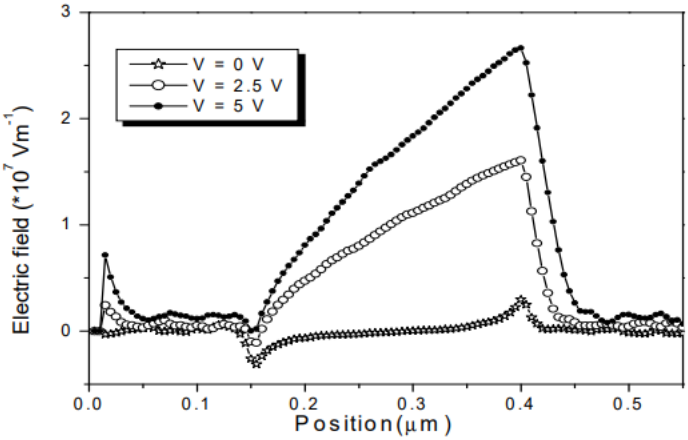

Figure 1. The electric field in the simulated SiC MOSFET for source-drain voltages between 0 and 5 V at room temperature

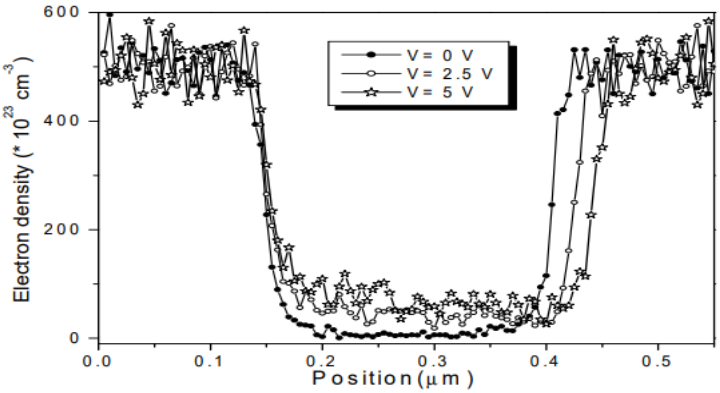

Figure 2. Electron density as a function of position in the model SiC MOSFET at room temperature for different source-drain voltages**.**

Figures 2 and 3 display the apparatus characteristics at room temperature while applying 5-volt voltage. A graph showing electronic free particle concentrations through the device is displayed in Figure 2. The device field speeds up incoming electrons through the buffer layer before they proceed to the drain. The formation of space charges becomes readily visible in Figure 3 because it indicates deviations from a uniform electric field. In Figure 3 we observe that the active layer achieves maximum drift velocity of 2.3 × 105 ms-1 when operating at 300 K. Electron transport behavior of SiC-based MOSFETs depends on gate length at 200 and 400nm during analysis shown in Figure 4. The figure presents data about drain-source voltage variations against drain current while altering gate lengths. When gate length reduces this graphic reveals how rising electric field strength and velocity overshoot conditions enable greater transport speeds. As a result, the electron transit time under the gate is decreased in two ways: The shortening of transit length happens simultaneously with velocity elevation. As electrons traverse the channel region beneath the gate they experience nearly ballistic acceleration because of the elevated field strength at the gate source termination.

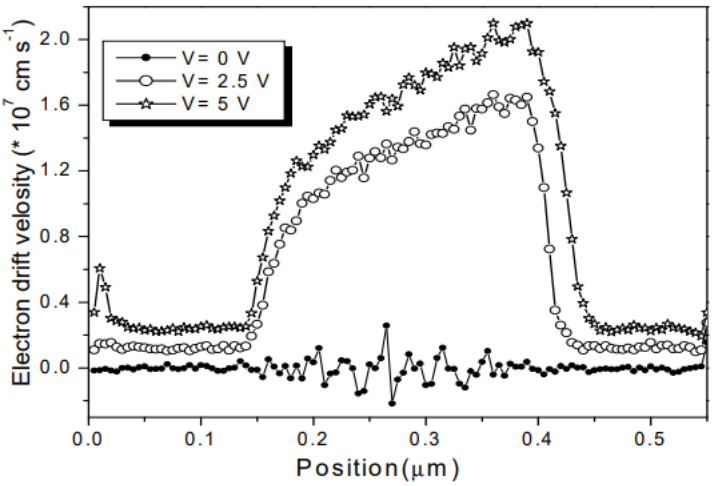

Figure 3. Electron drift velocity as a function of position in the model SiC MOSFET at room temperature for different source-drain voltages

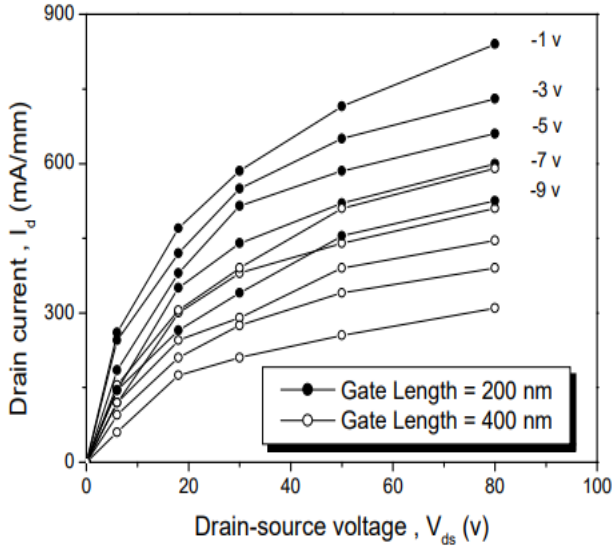

Figure 4. The effect of gate length on the electrical characteristics of SiC MOSFET. I-V characteristics for gate lengths of 200 and 400 nm has been illustrated

IV. Conclusion

It Researchers have studied how SiC MOSFET electron transport changes when gate length is used as a parameter. A reduction in gate length results in increased longitudinal electric field and velocity overshoot effects which lead I-V characteristics to show higher velocity performance.

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